

Fig. 1

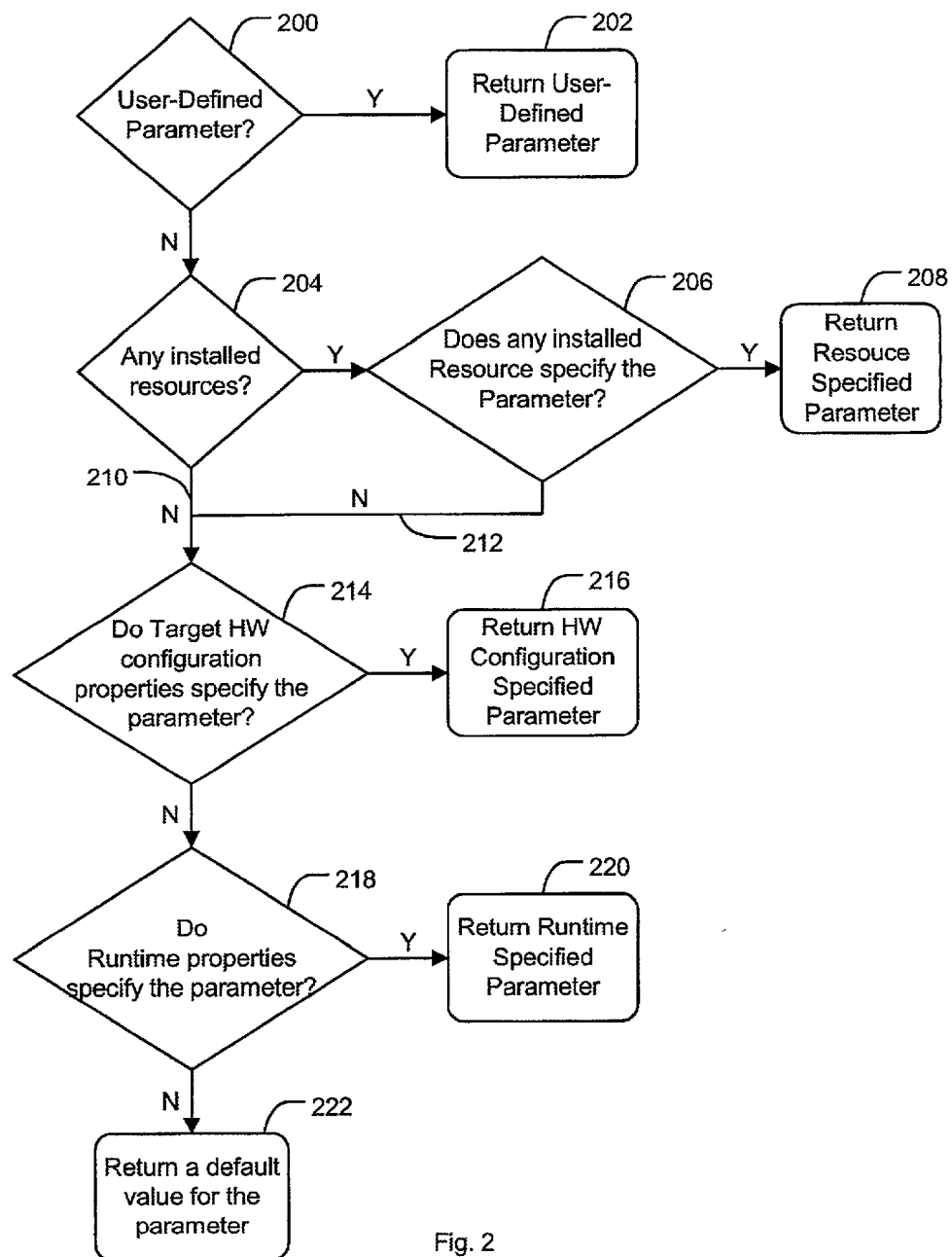


Fig. 2

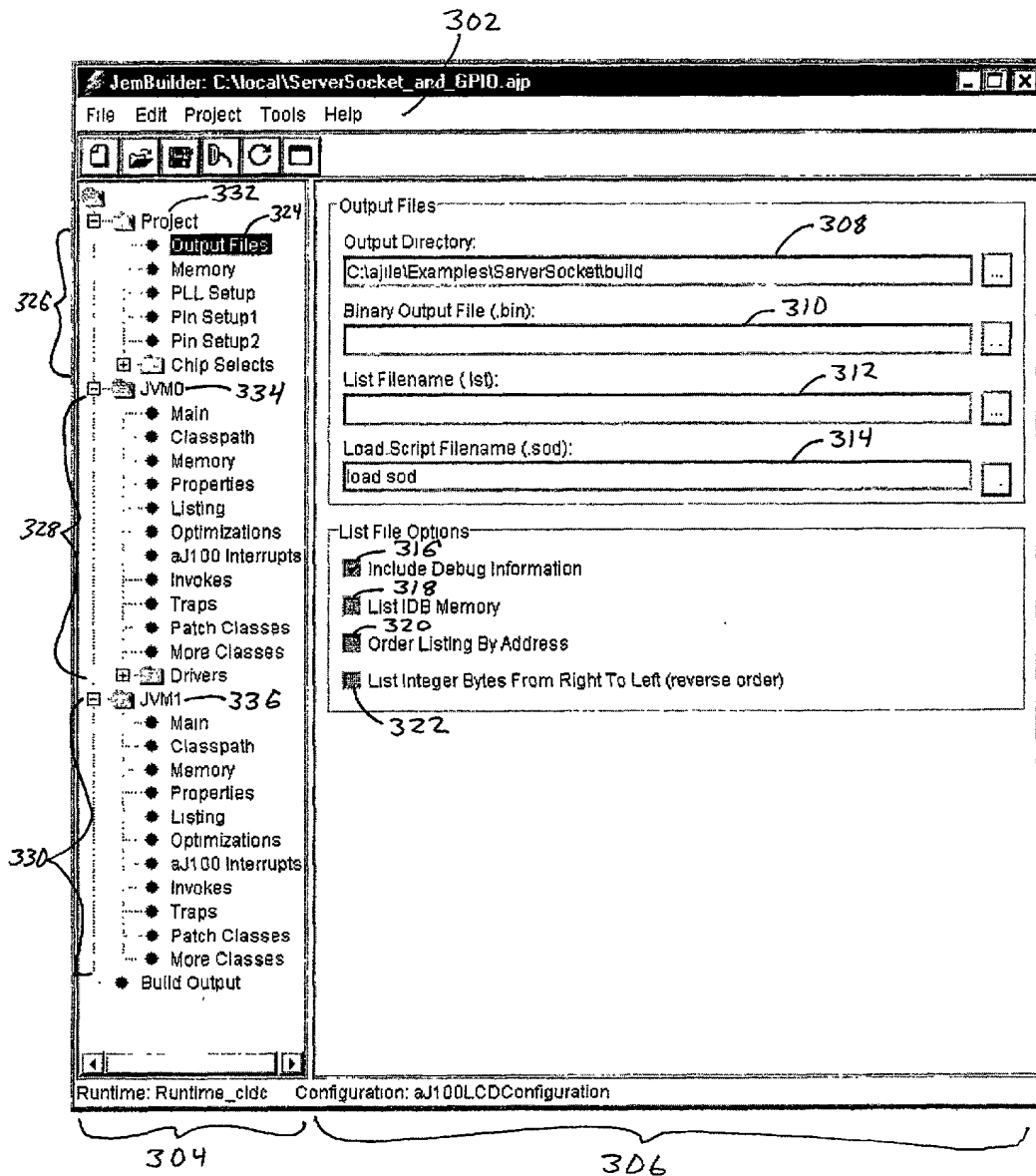


Fig. 3

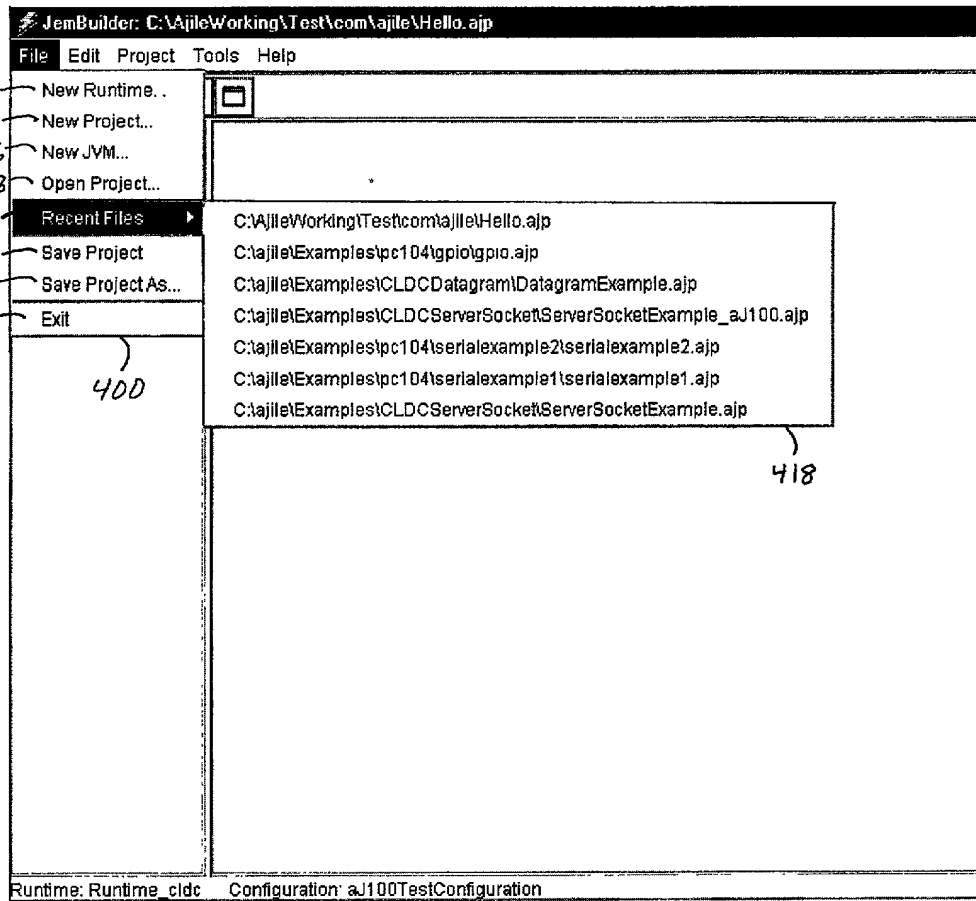


Fig. 4

New JVM step 1 of 4

Name

A Project can contain 1 or more JVM's. Each JVM runs independently, has its own memory, resources, and main method.
Each JVM has a name that is referenced in the navigation tree
Example: SystemJVM

Enter the name of the new JVM:

JVM2

Next > Cancel

502

← 500

Fig. 5

New JVM step 2 of 4

Main Class Name

Each JVM contains one entry point or main method. The package name must be specified followed by a '.' and the class name. This is called the fully qualified class name.
Example: com.example.Example

Enter the fully qualified class name:

GPIOMonitor

< Previous Next > Cancel

602

Fig. 6

600

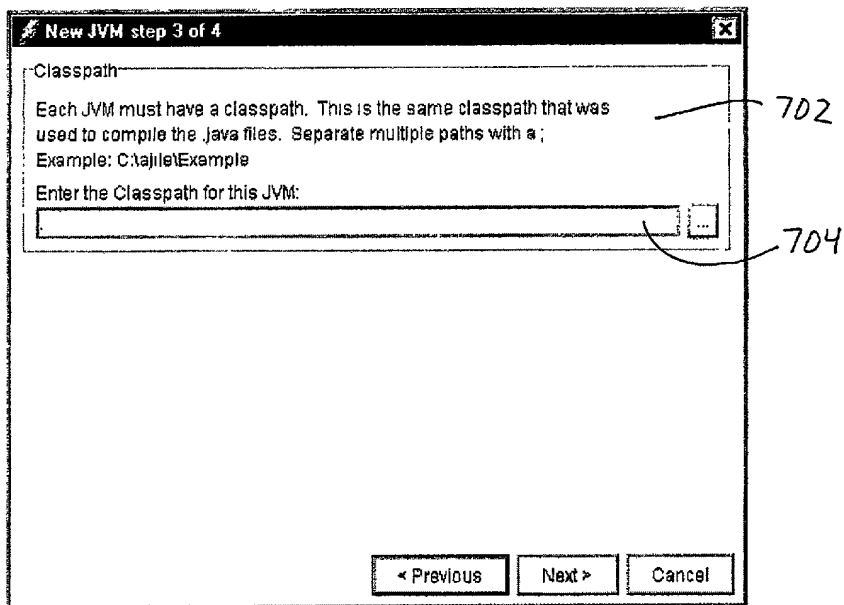


Fig. 7

700

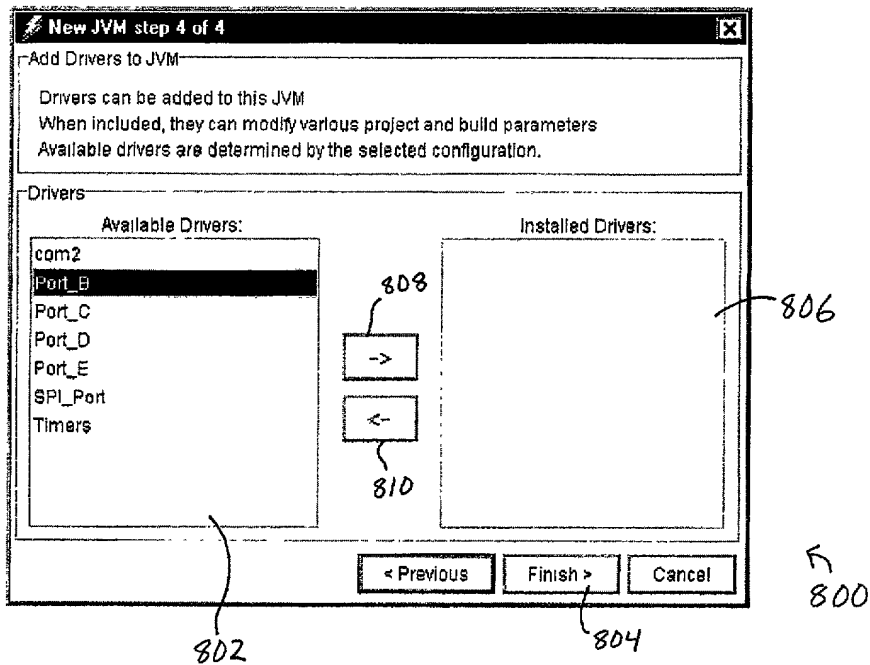


Fig. 8

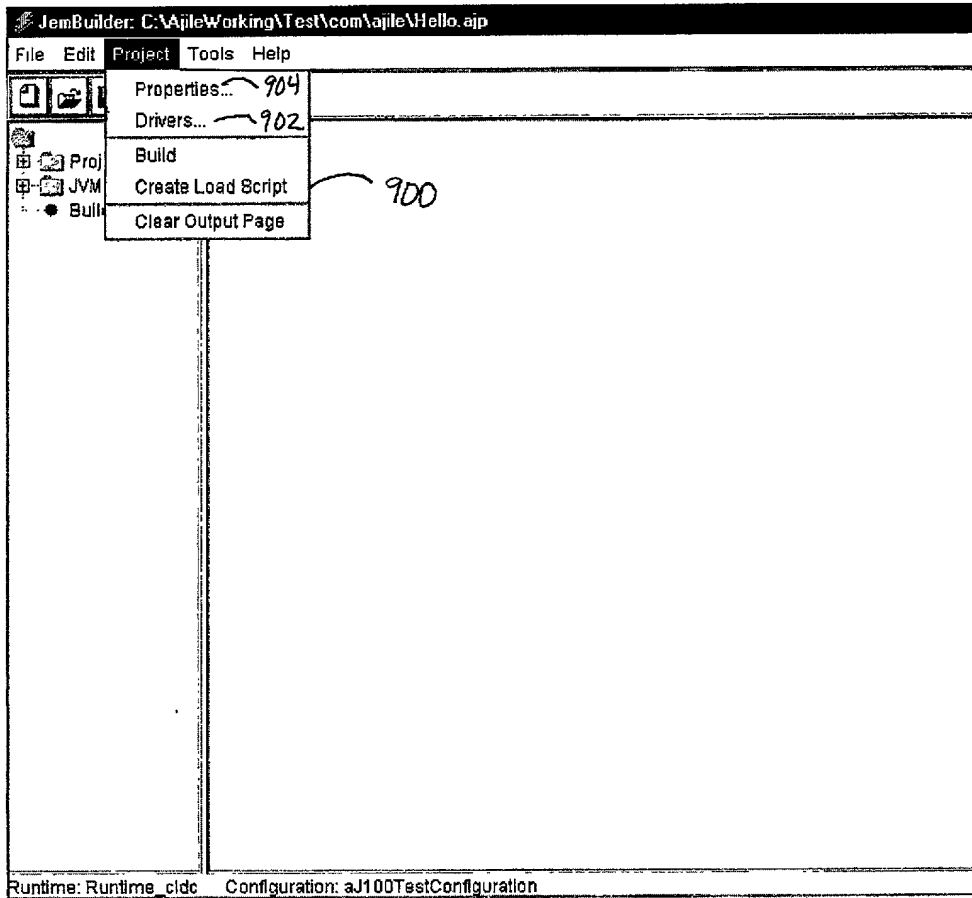
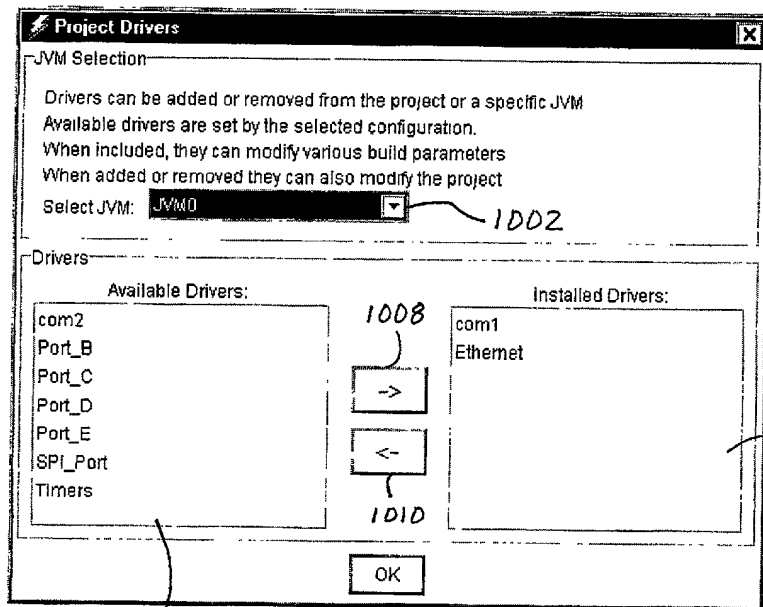


Fig. 9



1006

Fig. 10

~ 1000

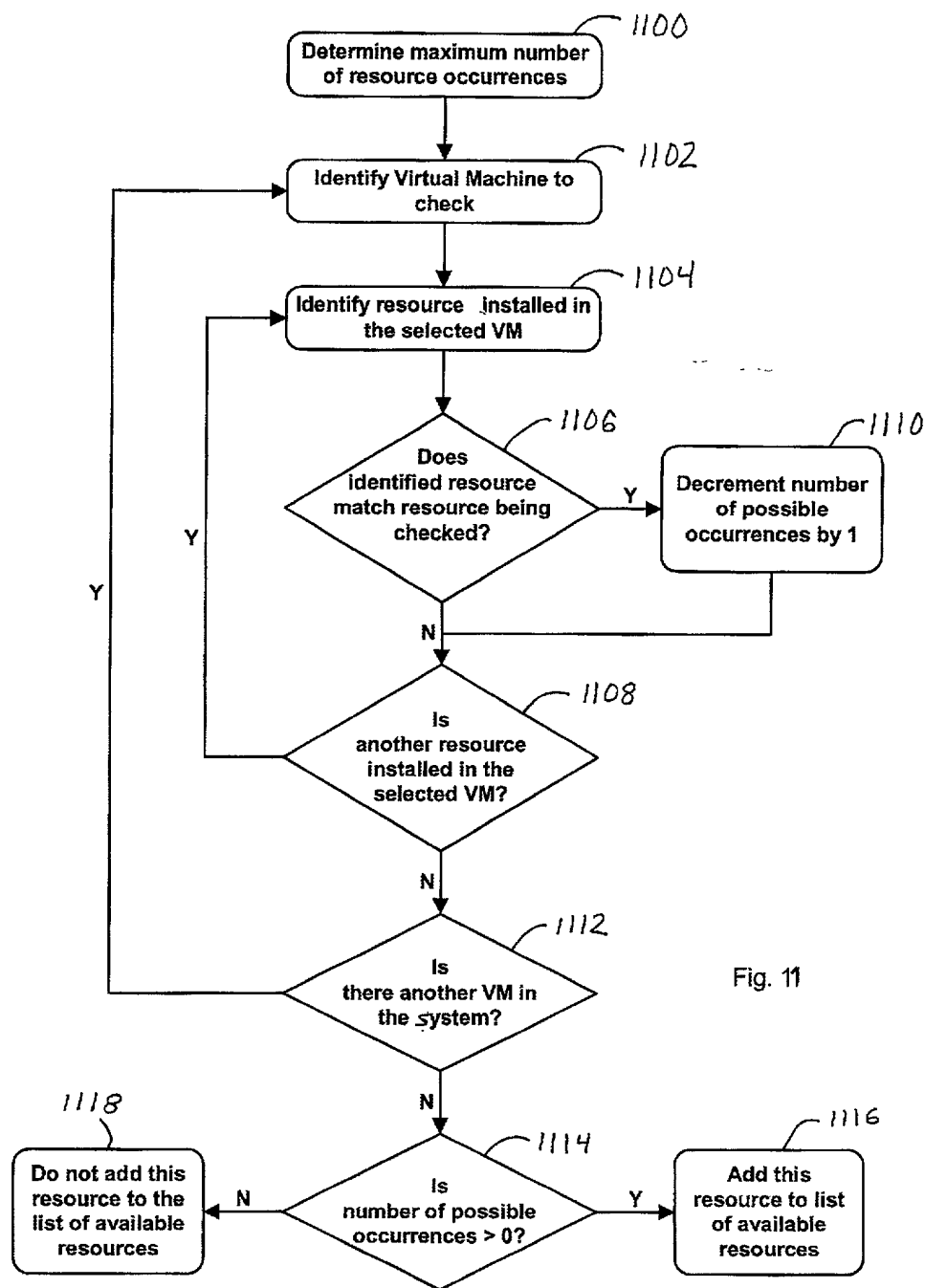


Fig. 11

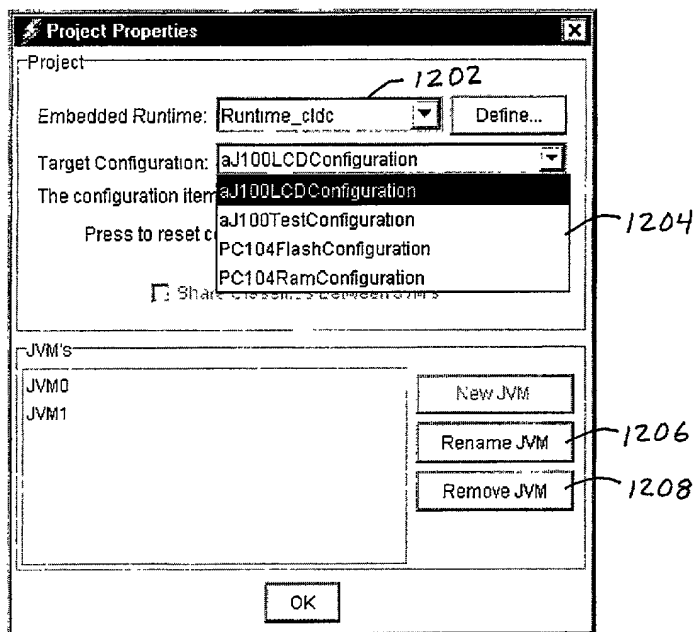


Fig. 12

1200

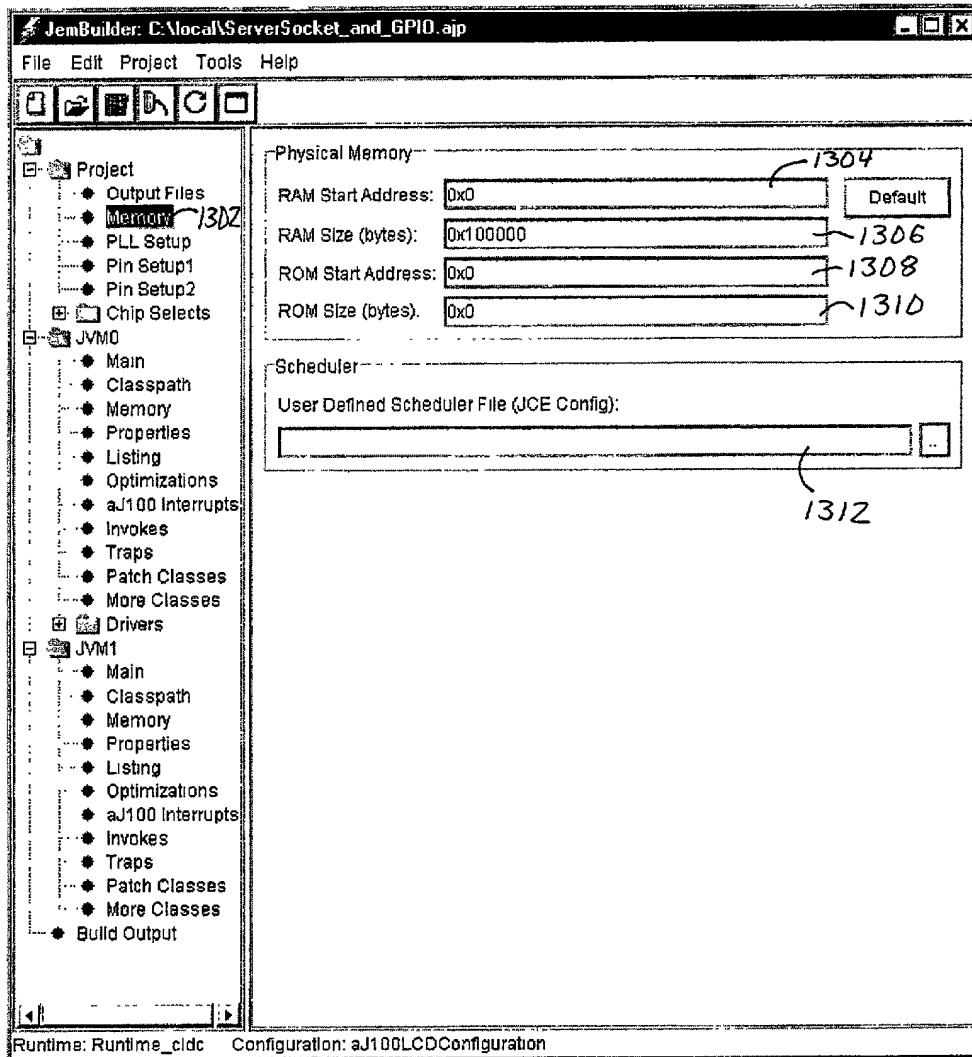


Fig. 13

1300

JemBuilder: C:\Local\ServerSocket_and_GPIO.apj

File Edit Project Tools Help

Project

- Output Files
- Memory
- PLL Setup**
- Pin Setup1
- Pin Setup2
- Chip Selects
- JVM0
 - Main
 - Classpath
 - Memory
 - Properties
 - Listing
 - Optimizations
 - aJ100 Interrupts
 - Invokes
 - Traps
 - Patch Classes
 - More Classes
- Drivers
- JVM1
 - Main
 - Classpath
 - Memory
 - Properties
 - Listing
 - Optimizations
 - aJ100 Interrupts
 - Invokes
 - Traps
 - Patch Classes
 - More Classes
 - Build Output

Phased Locked Loop Enable

☒ Enable PLL operation

The lock timeout can be used to bypass the PLL for a number of clock cycles, until the PLL stabilizes. The input clock will be used for the specified number of input clocks, then a switch is made to the PLL output. If the lock timeout is disabled, the PLL output will be used all of the time

3,670,016 Number of Cycles to PLL Driven Clock

Clock Frequency Calculation

10000000 Enter your input Clock Frequency in Hz

10 Select the PLL Multiplier

1 Select the PLL Divider

100000000 Internal Clock Frequency in Hz

48 Internal Time Prescaler

Clock Out Frequency

The Clock Out pin can be disabled, or its frequency divided down

2 Select the Clock Output Divider

50000000 Clock Out Frequency in Hz

Runtime: Runtime_cide Configuration: aJ100LCDConfiguration

Fig. 14

 κ_{1400}

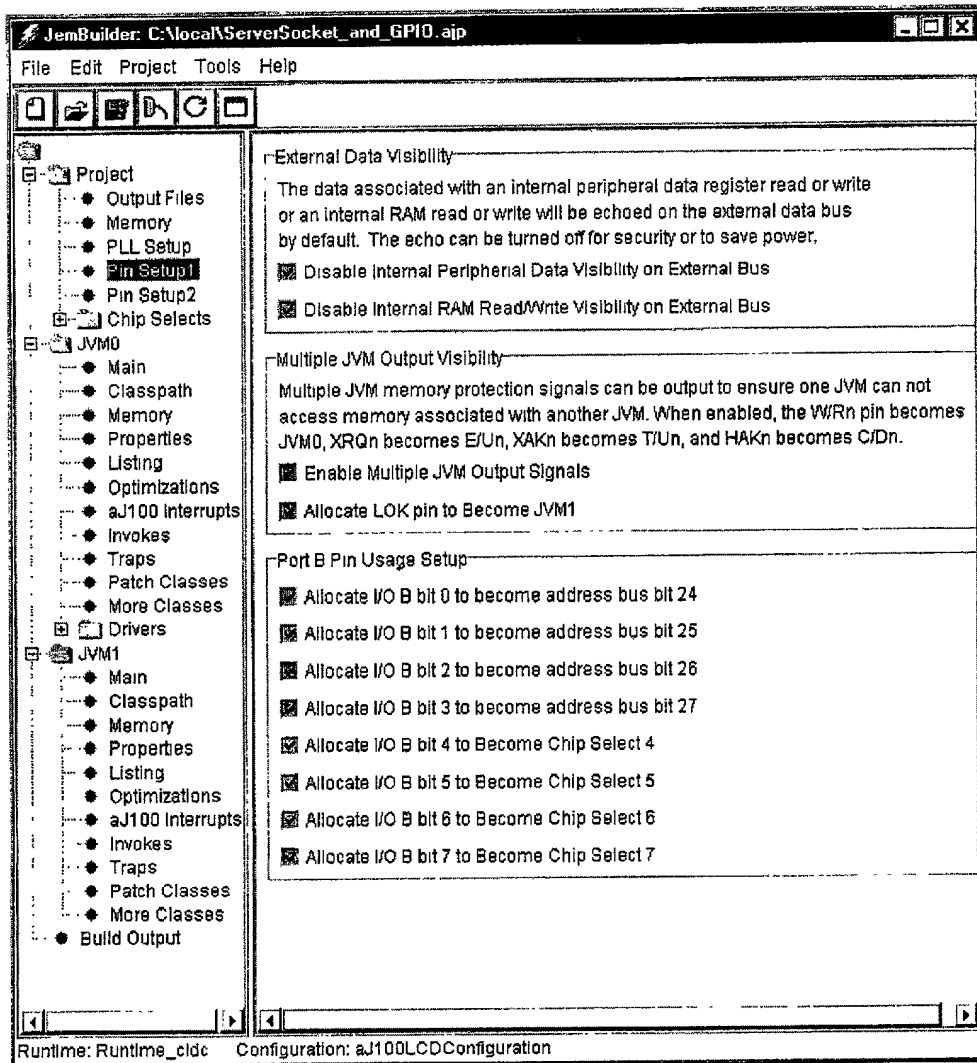


Fig. 15

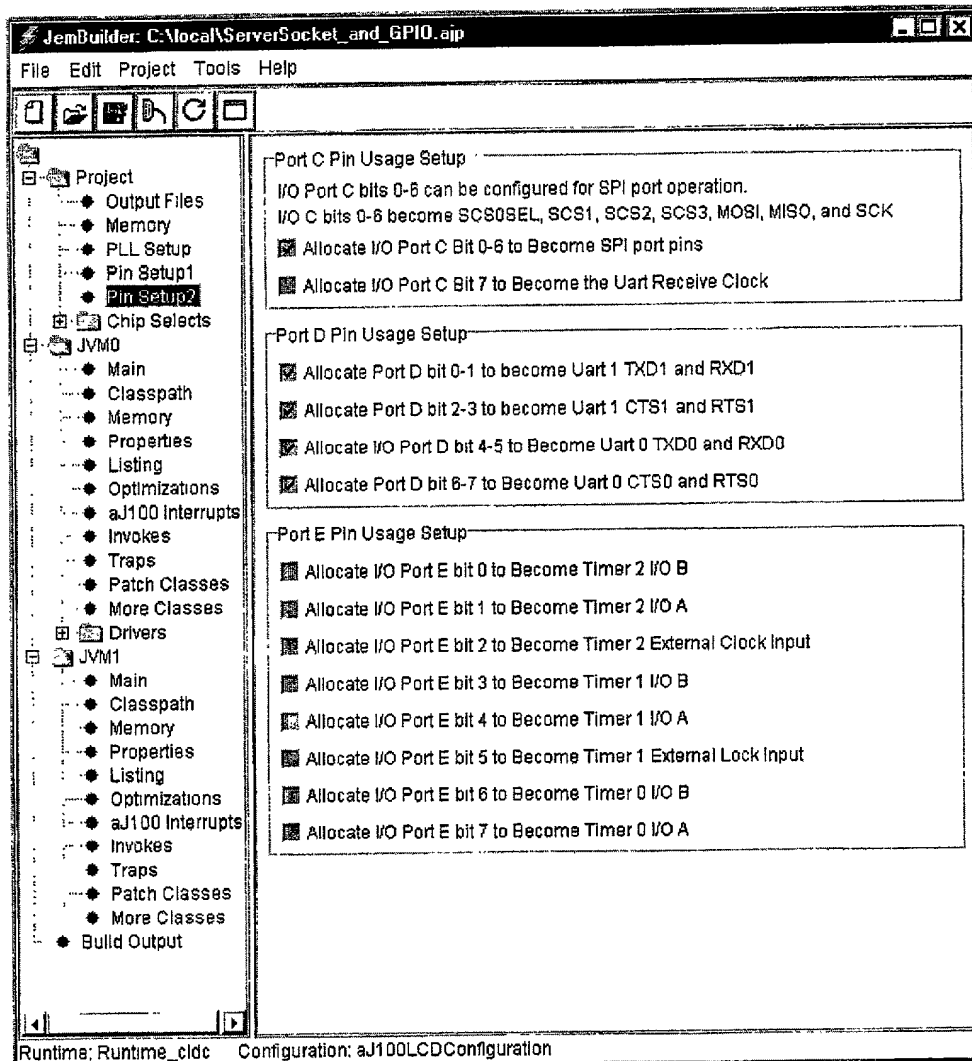


Fig. 16

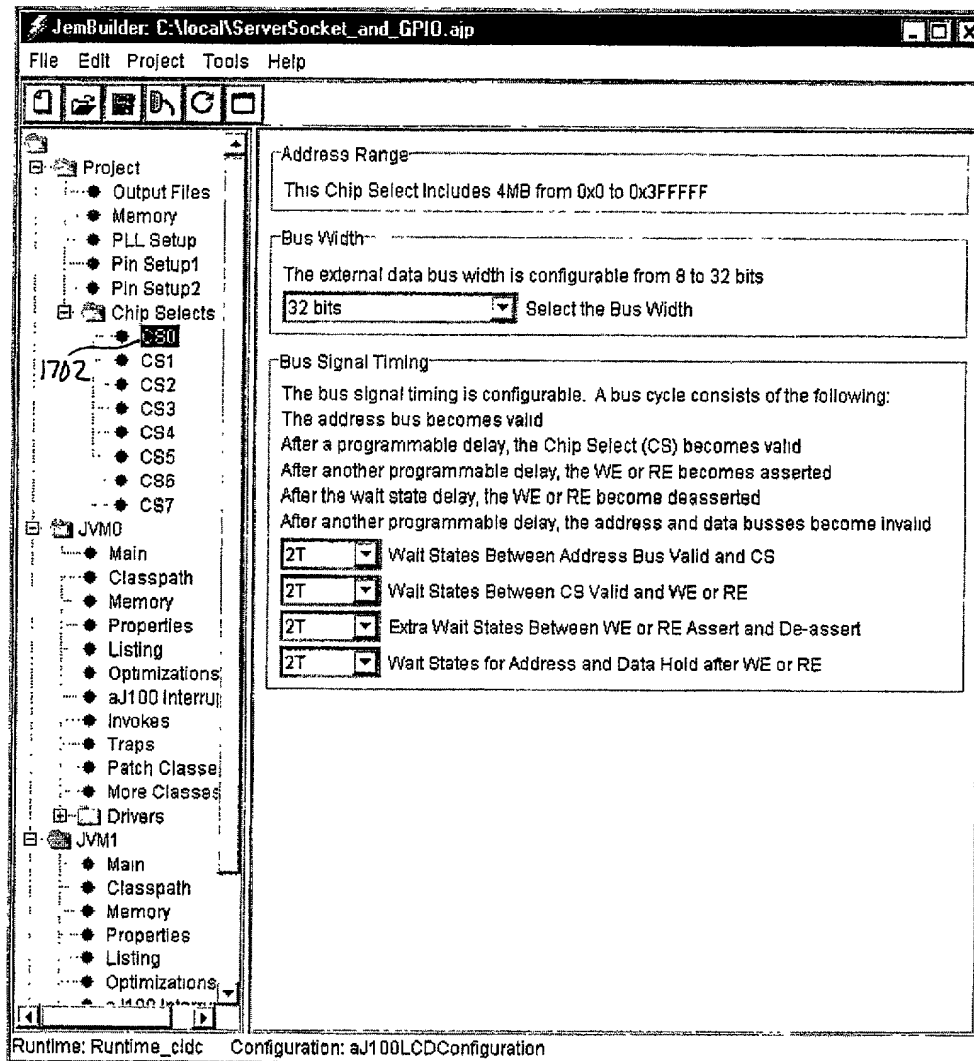


Fig. 17

1700

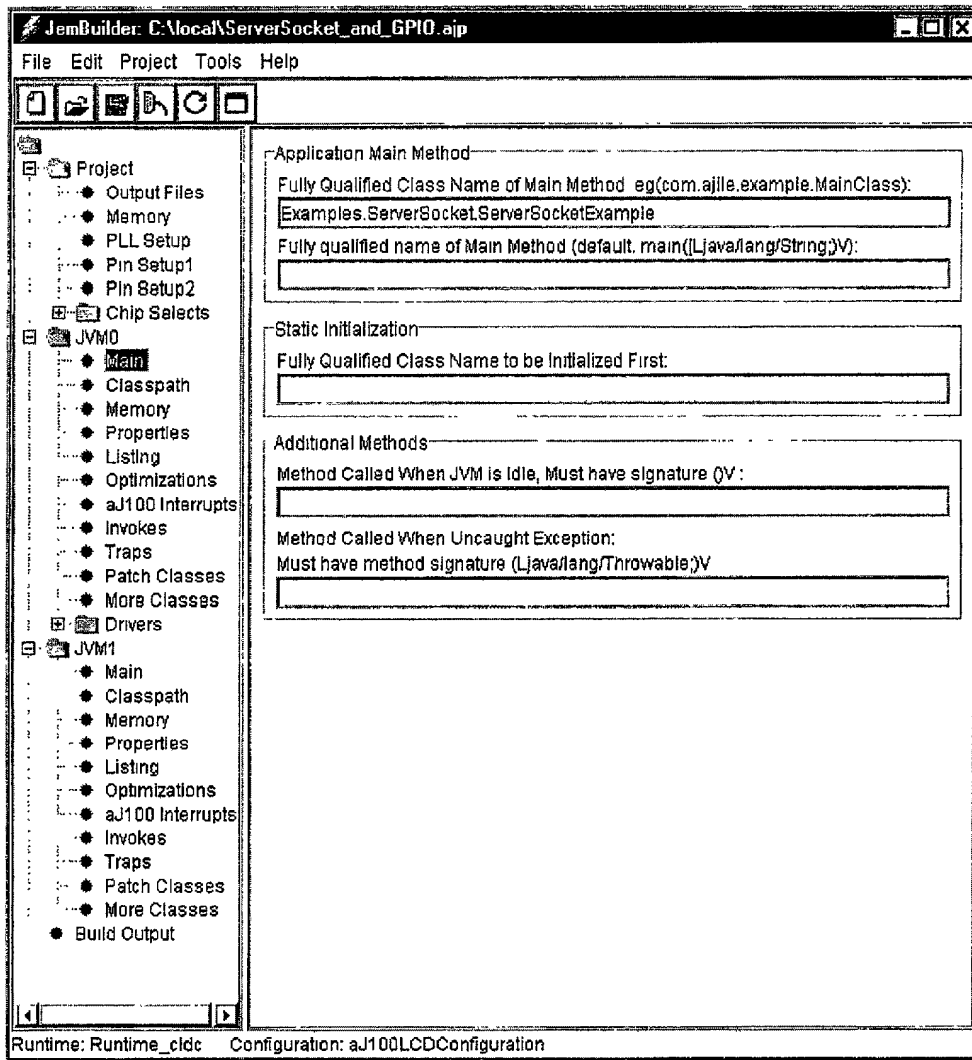


Fig. 18

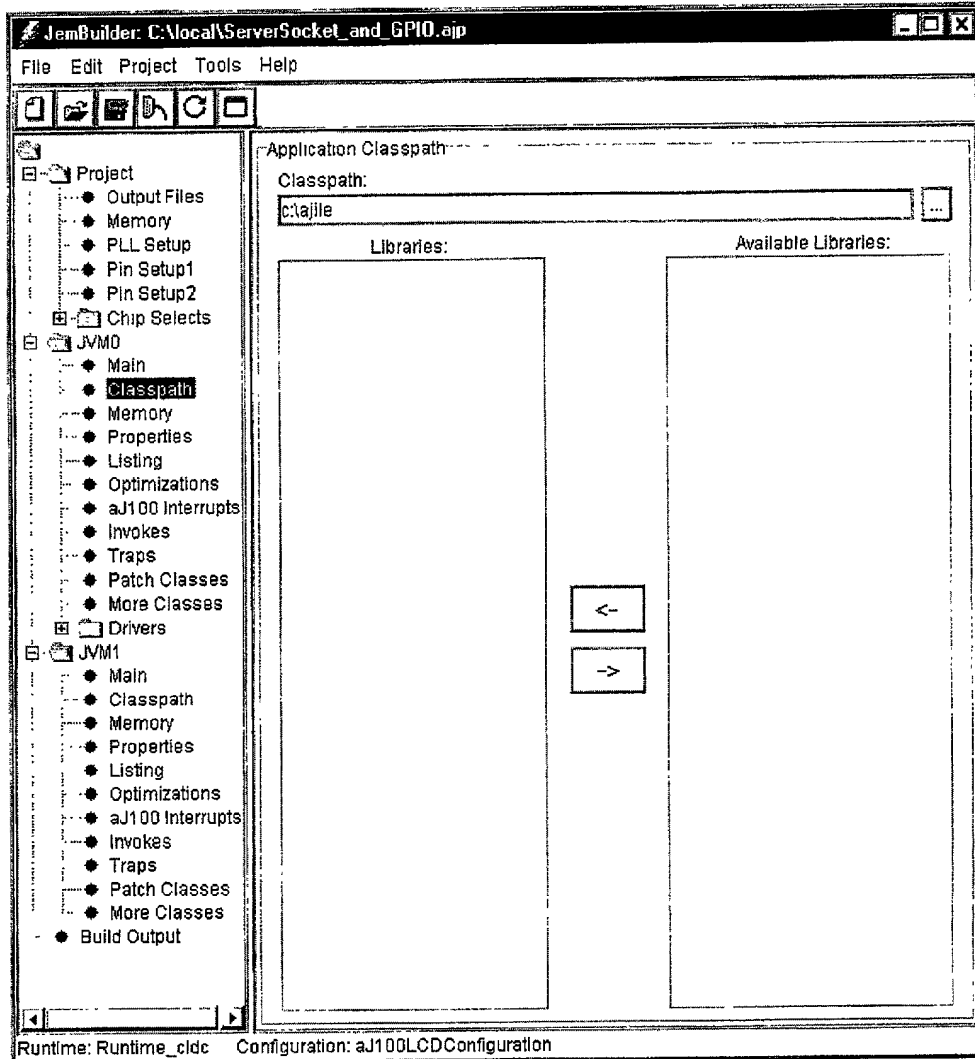


Fig. 19

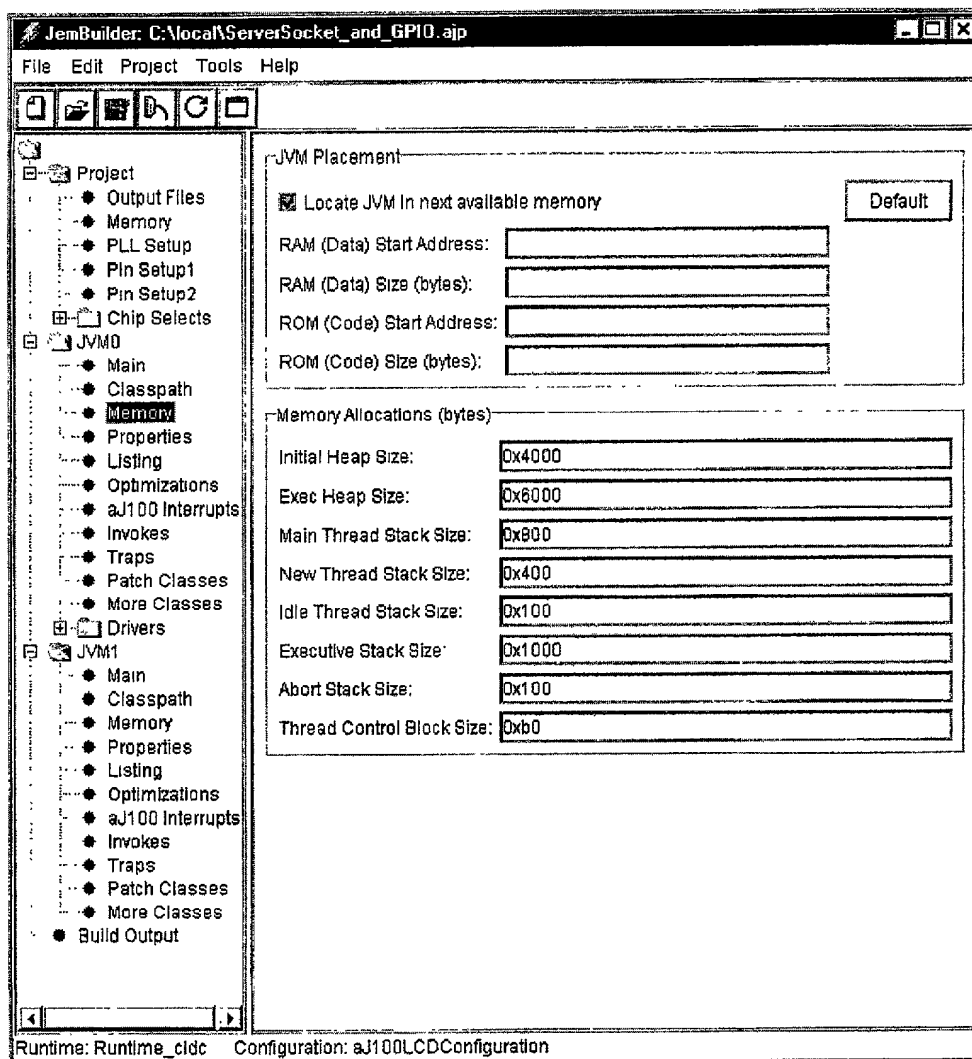


Fig. 20

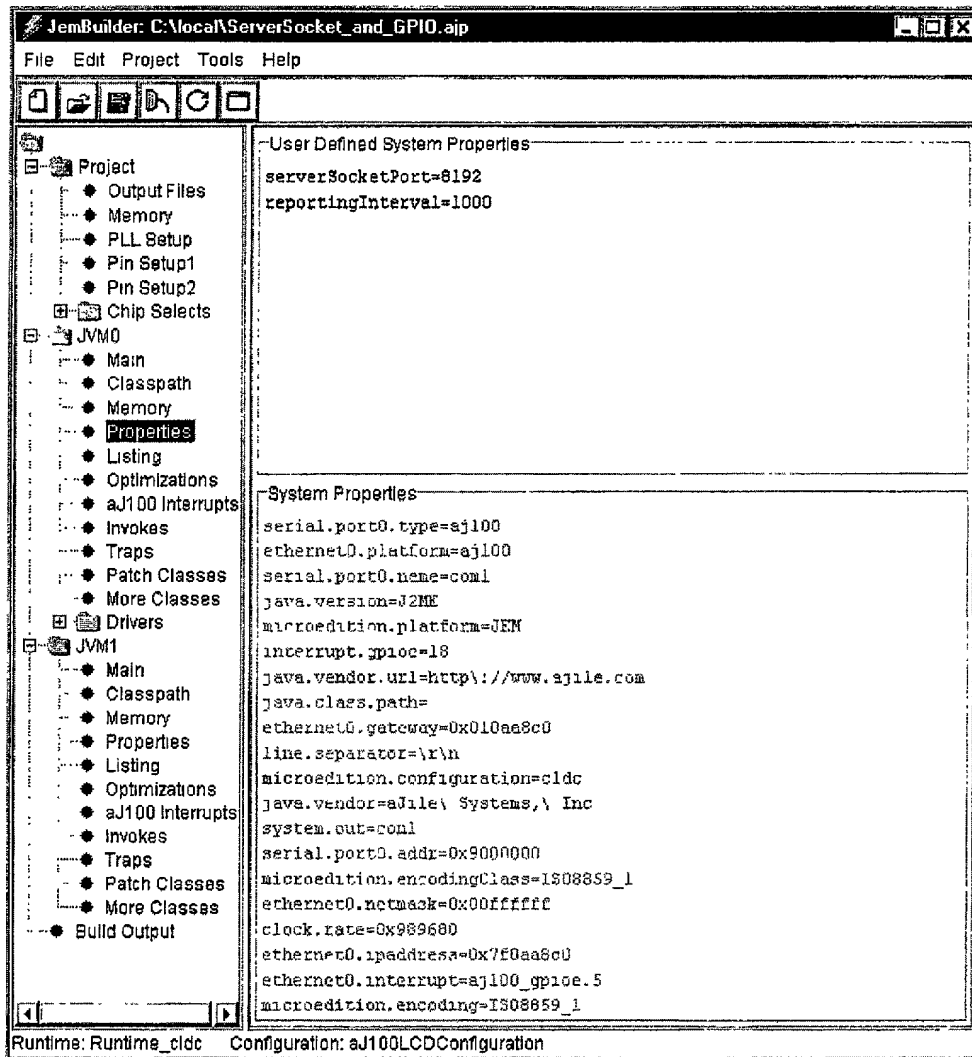


Fig. 21

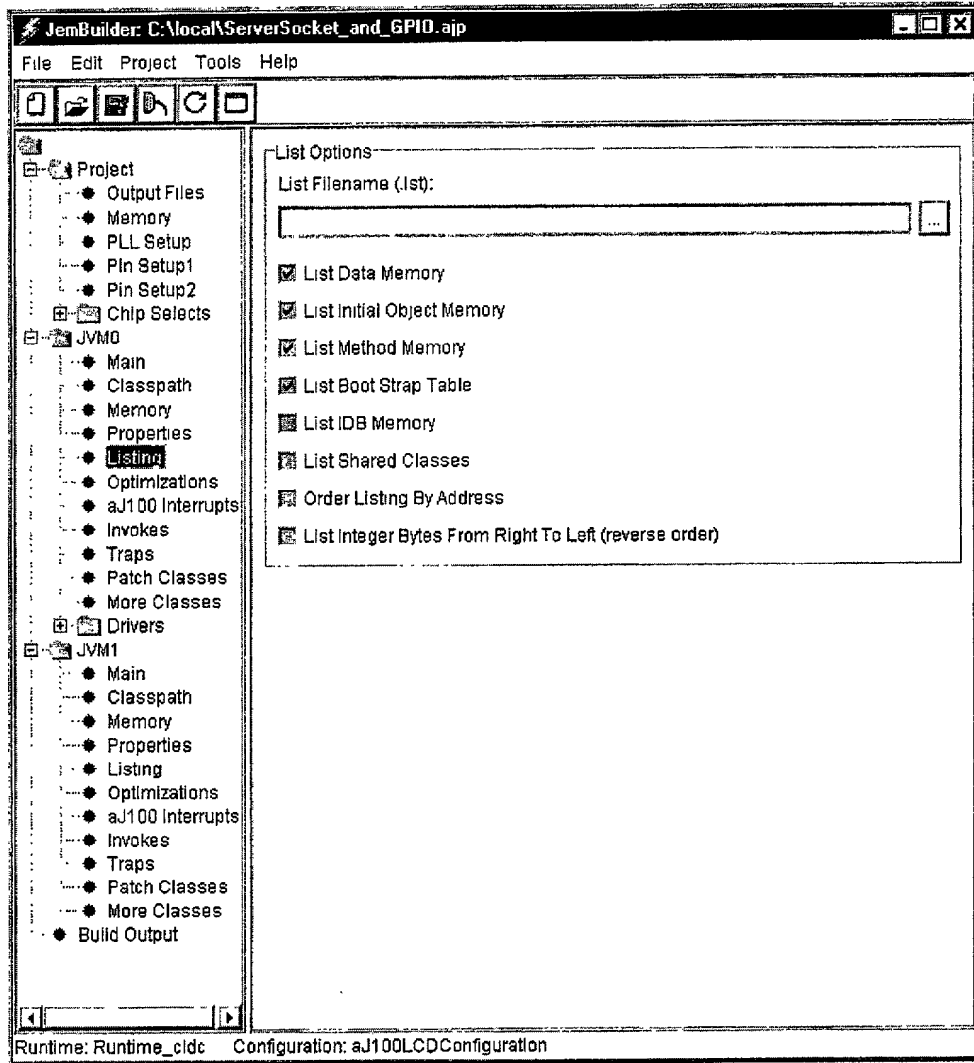


Fig. 22

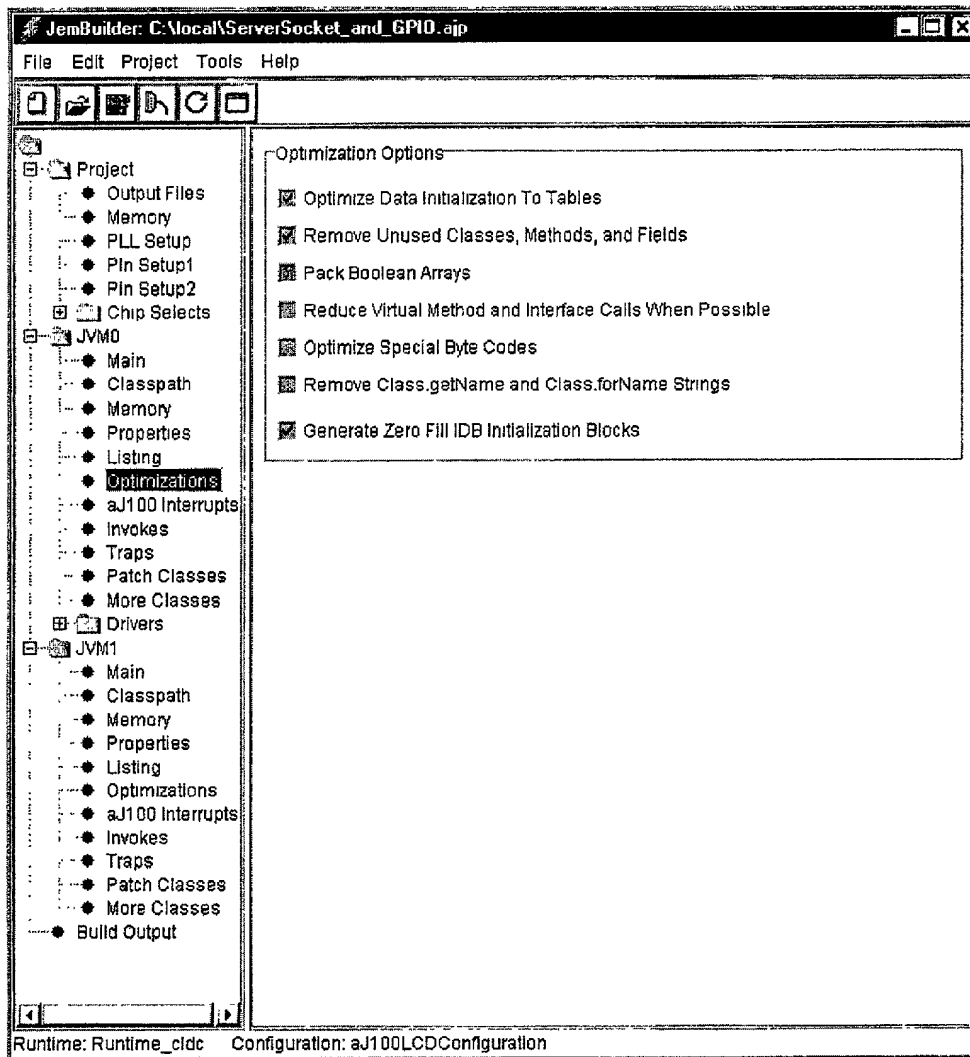
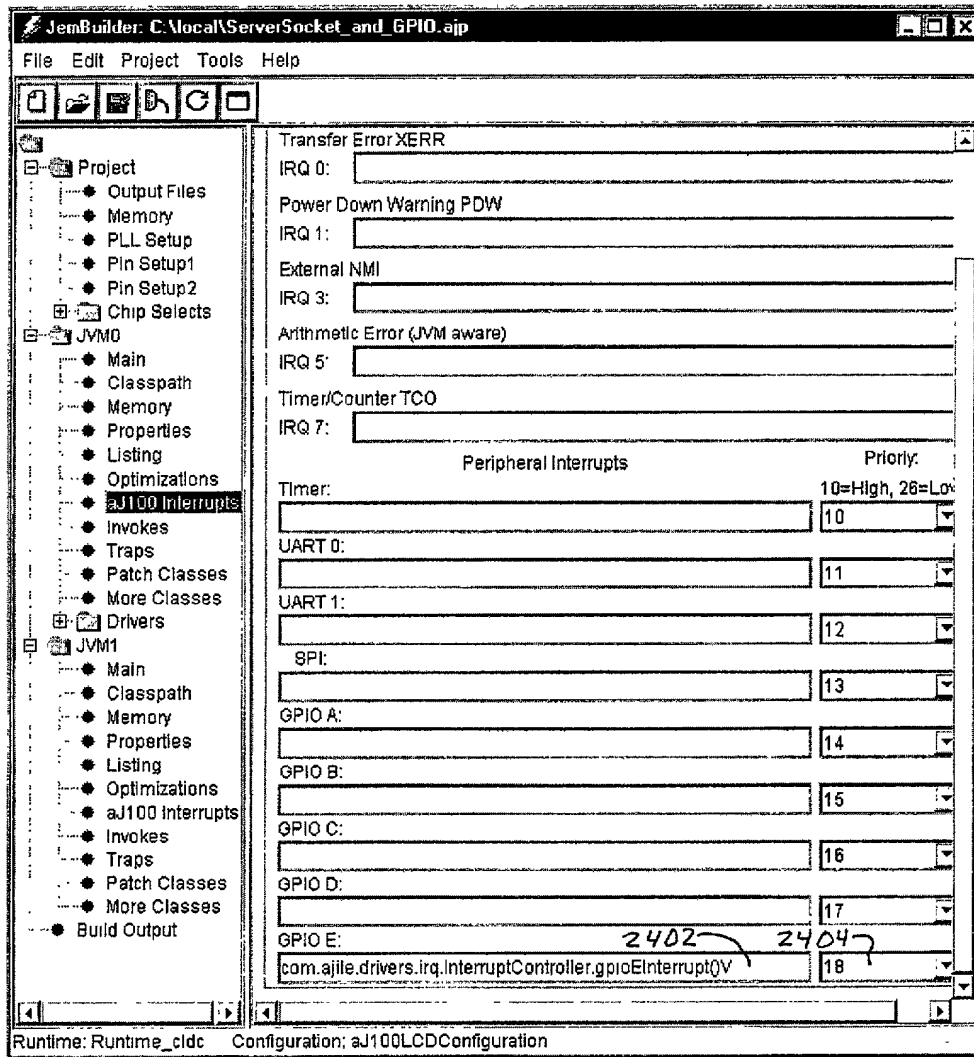


Fig. 23



2400 →

2406

Fig. 24

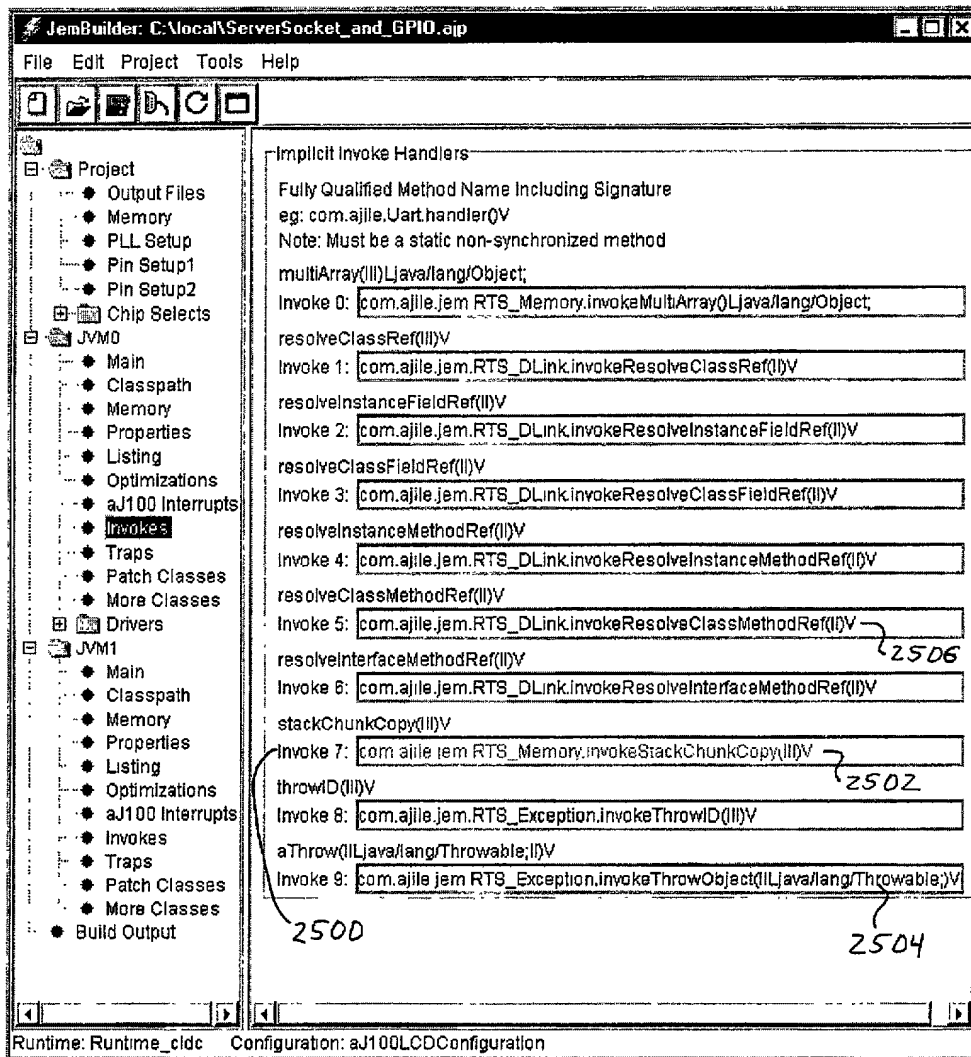


Fig. 25

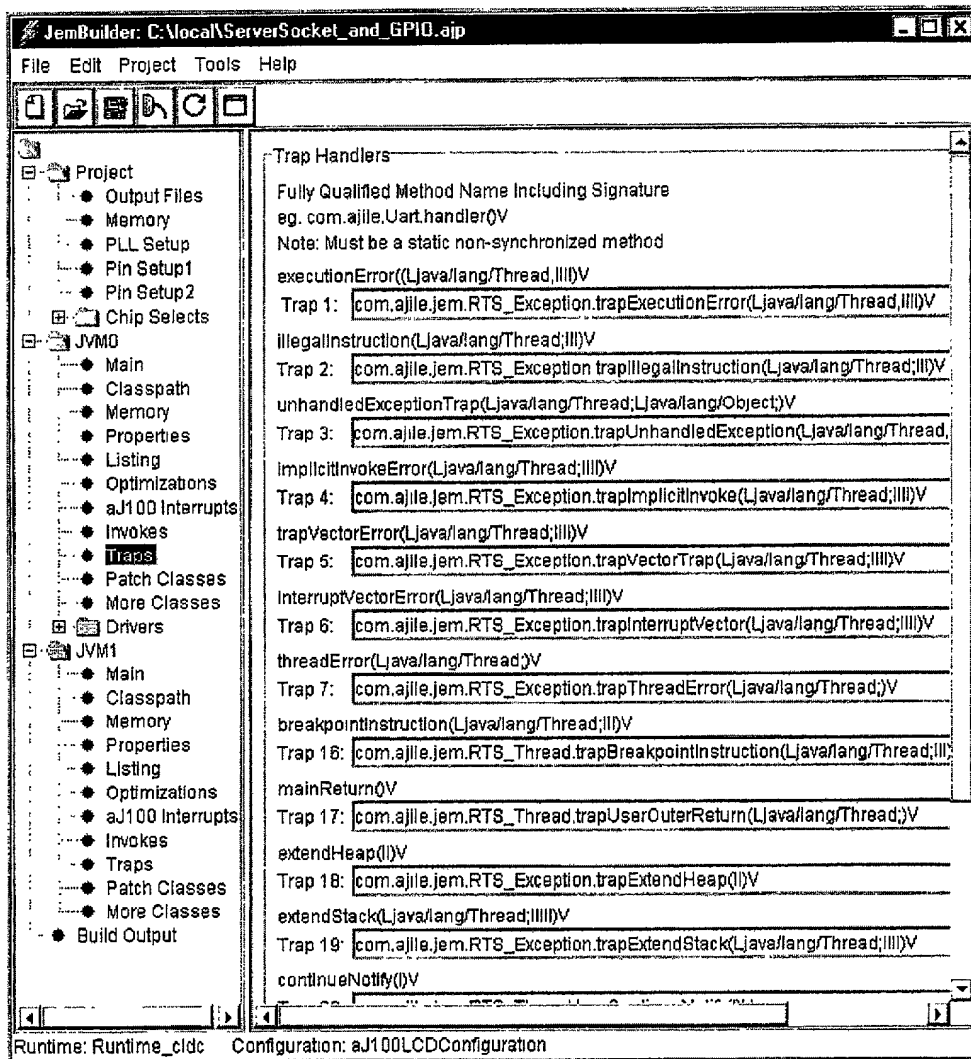


Fig. 26

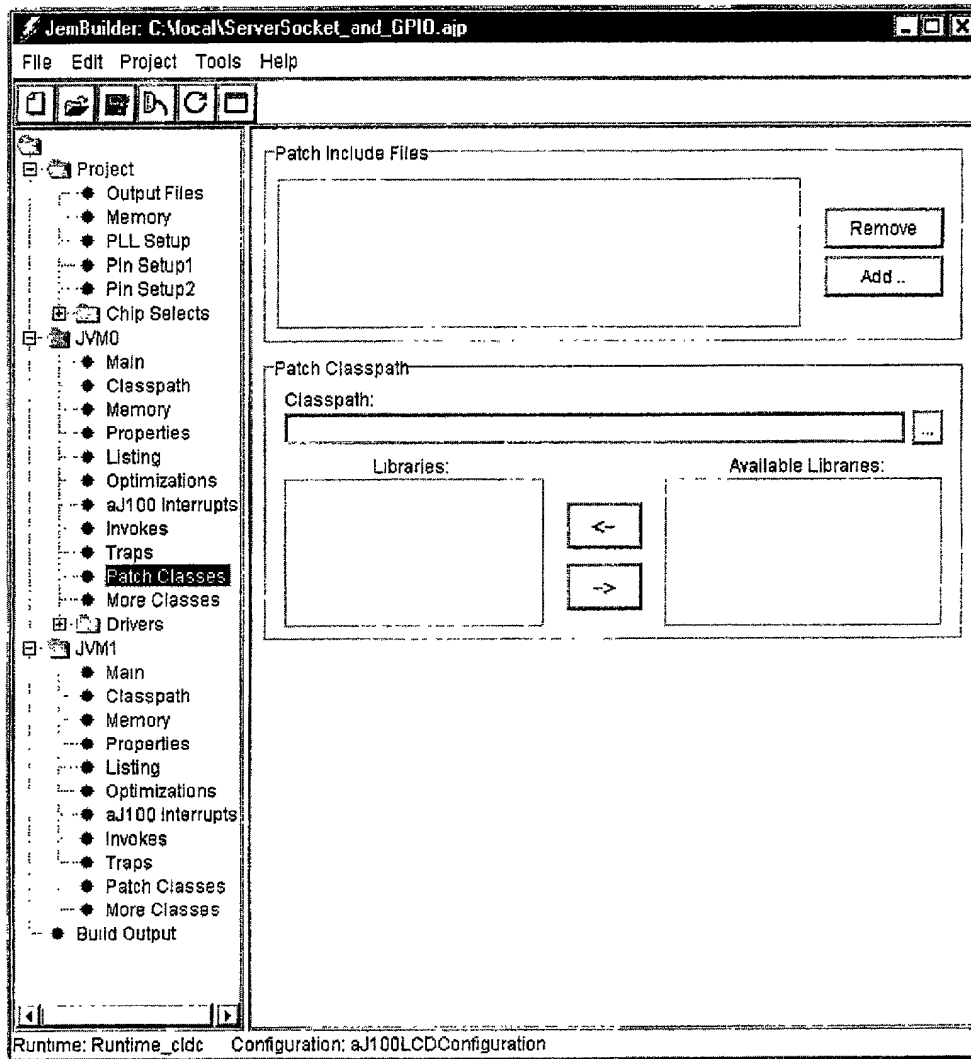


Fig. 27

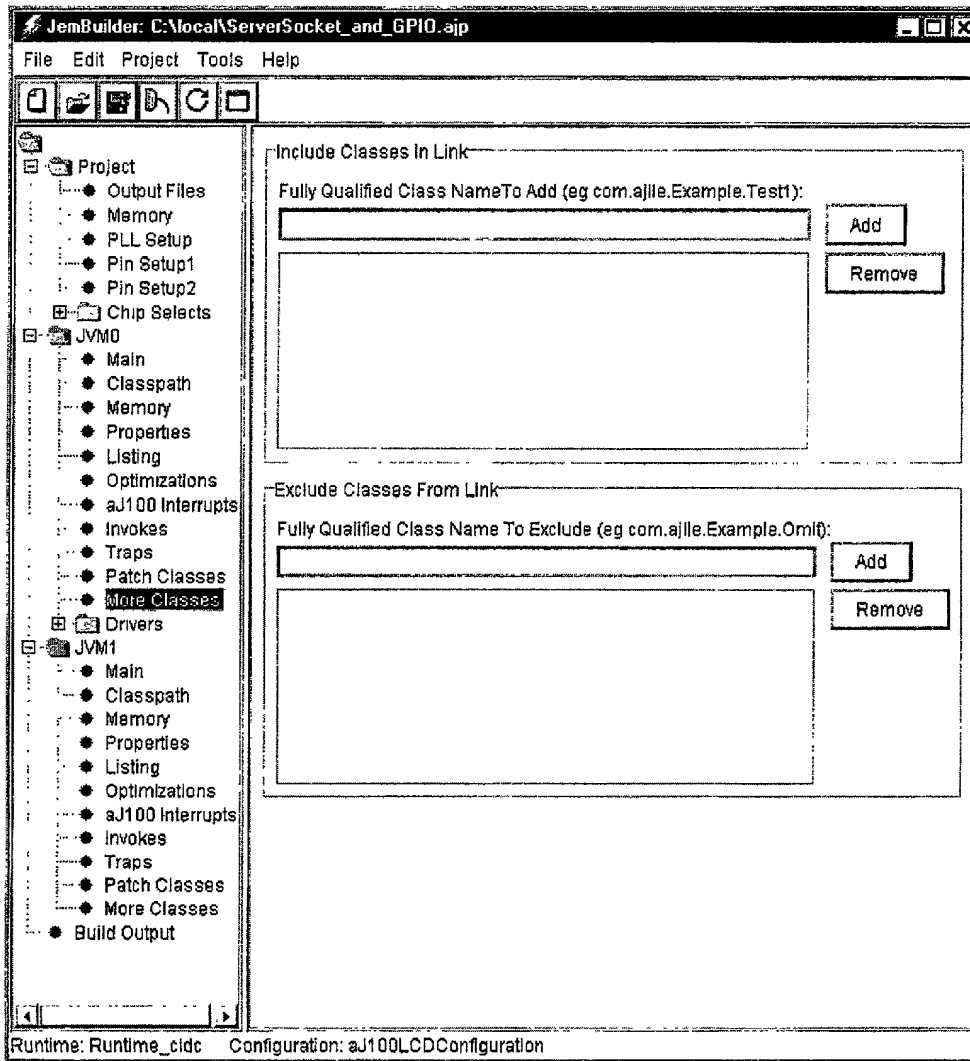


Fig. 28

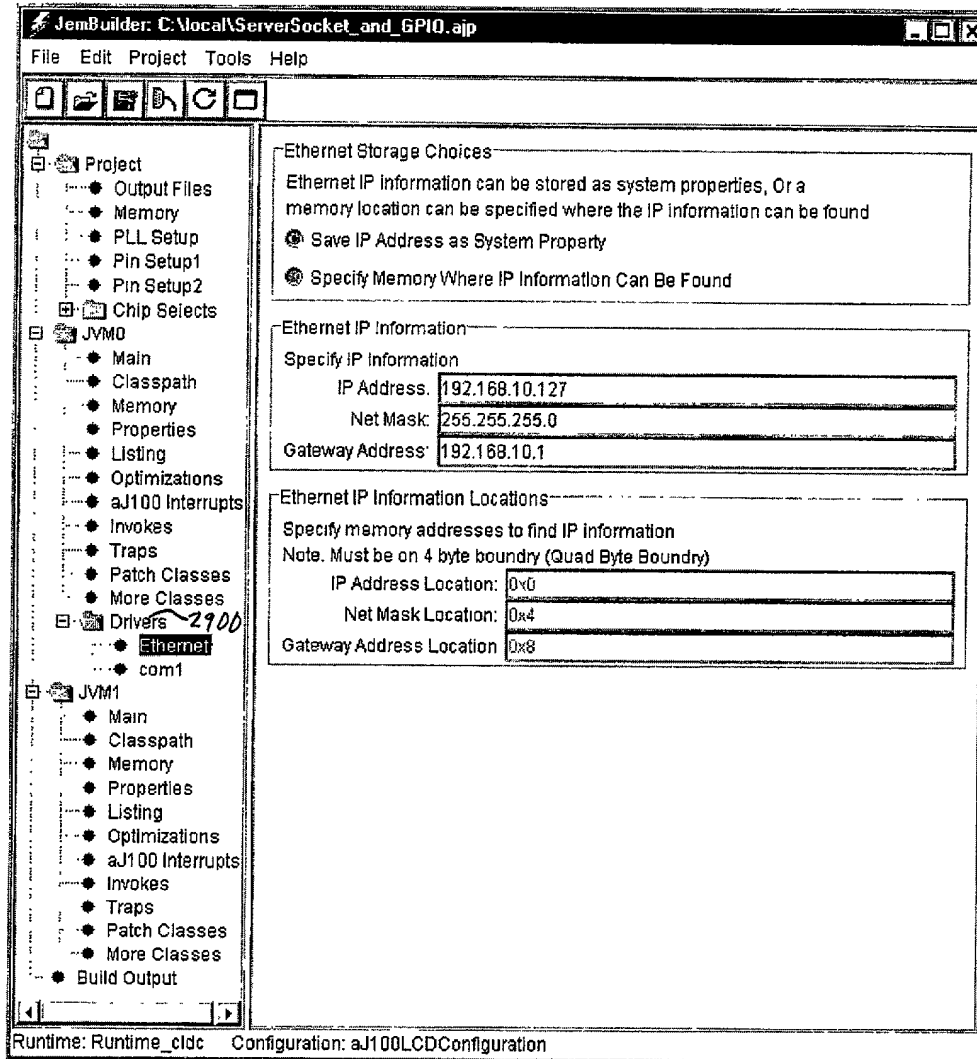


Fig. 29

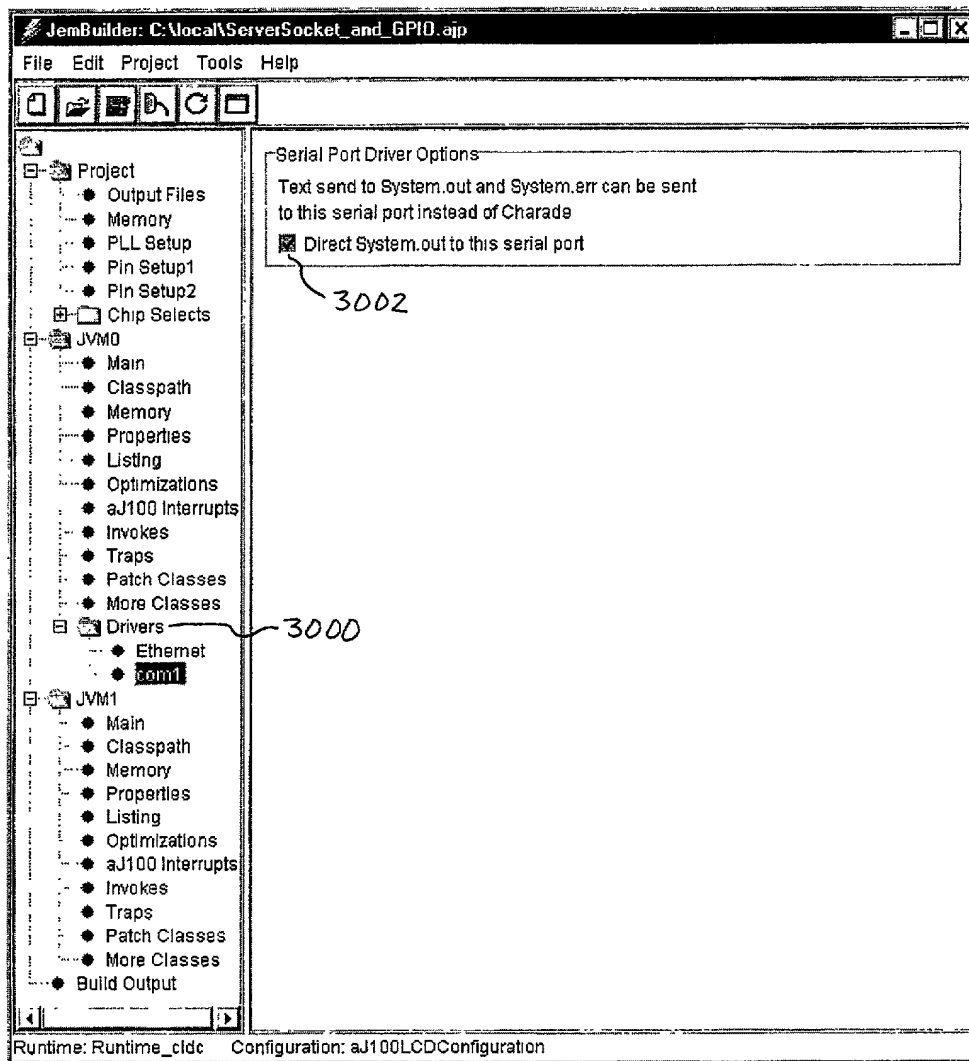


Fig. 30

Patented 6,941,890

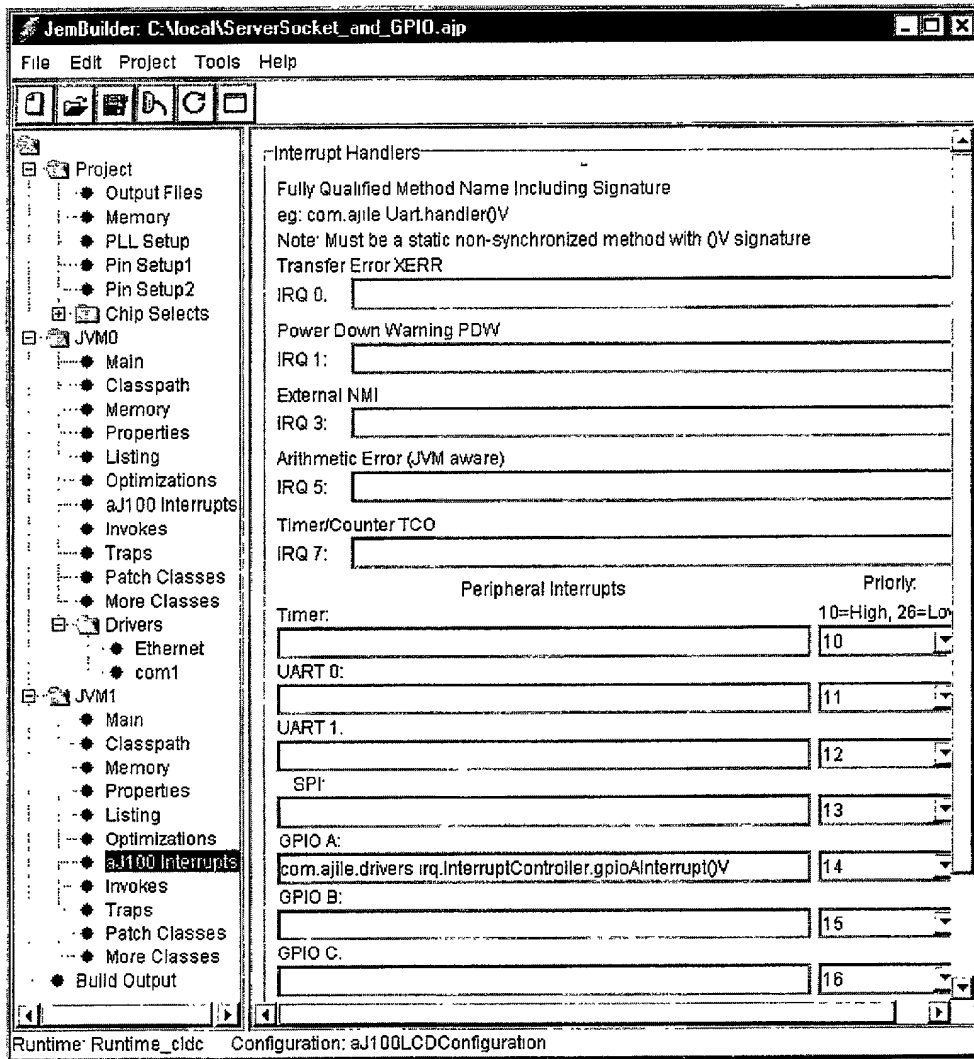


Fig. 31